Frequency Resolution

The iMS4 employs the AD9959 direct digital synthesizer chip operating from a system clock (SysClk) of 491.52MHz. The output RF frequency is derived from this system clock with 16bit resolution, scaled across the iMS4 output frequency range of 12.5MHz to 200.66MHz.

1: Frequency resolution = 49/128 x SysClk / 2^16 = 2.871138KHz

Output frequency = 12.5 + (0.002871138 x N) MHz …….(1)
where N = 0 - 65535

Inherently, the AD9959 is capable of 32-bit resolution however to maximize point to point update rate for frequency scanning applications, the lower resolution of 16-bits is applied. This is more than adequate for acousto-optic applications. Nevertheless, for single tone applications it is still possible to program all 32bits of frequency using the *DDSScript* function in the SDK. Note: this feature is not available through the Isomet GUI.

Phase Locking

A separate PLL circuit locks the DDS system clock (SysClk) to an external reference clock (ERC) input applied to connector J8. The iMS4 firmware generates a (PLL) lock signal when locked. This can be assigned to one of the front panel LEDs by adapting the *StartupConfiguration* from the SDK.

External reference (ERC)

By default, the PLL reference clock input is connected to an internal 25MHz TCXO.
Alternatively, an external reference clock on pin 2 (sig) / pin 1 (rtn) of J8 can be applied.

The ERC input requires a positive going digital signal and is 50ohm terminated.
The signal is routed to a 5V tolerant buffer and then a digital isolator. The buffer and digital isolator operate from an isolated 5V supply which the user needs to provide on pin 21 (+5V) / pin 17 (0V) of J8.

Reference Clock:

Frequency: any multiple of 20KHz …….(2)
Minimum 40KHz, Maximum 16MHz

Voltage: Positive only, 50ohm input impedance
Minimum 1.25V, Maximum 5.0V

Viewing Lock on an Oscilloscope

To see stationary traces on a scope will require an exact integer relationship between the ERC reference and the output RF frequency with due consideration of the resolution limitations given by (1) and (2) above.
(Even so, there will be a very slow drift of ~26 second period due to finite (32bit) resolution of the DDS.)

One solution is to apply an ERC of 2.5000MHz and program an output frequency of 12.5000MHz